M68000PM/AD
REV. 1

PROGRAMMER'S REFERENCE MANUAL

(Includes **CPU32** Instructions)

MOTOROLA

Introduction 1

Addressing Capabilities 2

Instruction Set Summary 3

Integer Instructions 4

Floating Point Instructions 5

Supervisor (Privileged) Instructions 6

CPU32 Instructions 7

Instruction Format Summary 8

Processor Instruction Summary A

Exception Processing Reference B

S-Record Output Format C

PREFACE

This manual contains detailed information about the software instructions used by the microprocessors and coprocessors in the M68000 family. The manual is organized as follows:

Section 1 Introduction—This section contains information on the M68000 family programming model, register description, integer and floating-point data formats and data types as well as information on format organization in registers and memory. Also included is a table of notational conventions used throughout this manual.

Section 2 Addressing Capabilities—This section presents detailed information on the format of instructions and their various bit field definitions and possible encodings. Also included are descriptions of addressing modes and other data structures used by the M68000 family.

Section 3 Instruction Set Summary—This section includes extensive information on the instruction set (grouped by operational category), descriptions of the operands used by instructions, and guidelines on how to use the instructions.

Section 4 Integer Instructions—This section provides all integer instruction (nonprivileged) operations described in detail and organized alphabetically.

Section 5 Floating-Point Instructions—This section provides all nonprivileged floating-point instruction operations described in detailed and organized alphabetically.

Section 6 Supervisor (Privileged) Instructions—This section provides all privileged instruction operations described in detail and organized alphabetically.

Section 7 CPU32 Instructions—This section provides all CPU32 instruction operations described in detail and organized alphabetically.

Section 8 Instruction Format Summary—This section contains all the M68000 instruction formats (binary), arranged by opcode.

Appendix A Processor Instruction Summary—This section contains a table listing of all the M68000 family instructions arranged alphabetically and cross-referenced to show which instructions are applicable to which processors. Each processor is also listed with a table of the instructions and the addressing modes that apply to that processor.

Appendix B Exception Processing Reference—This section presents information on exception vector assignments for the M68000 family and illustrations of exception stack frames and floating-point stack frames.

Appendix C S-Record Format—This section provides detailed information on the S-record format.

TABLE OF CONTENTS

Paragraph Number	Title	Page Number
	Section 1 Overview	
1.1	Integer Unit User Programming Model	1-2
1.1.1	Data Registers (D7–D0)	1-2
1.1.2	Address Registers (A7–A0)	1-2
1.1.3	Program Counter	1-3
1.1.4	Condition Code Register	1-3
1.2	Floating-Point Unit User Programming Model	1-4
1.2.1	Floating-Point Data Registers (FP7–FP0)	1-4
1.2.2	Floating-Point Control Register (FPCR)	1-5
1.2.2.1	Exception Enable Byte	1-5
1.2.2.2	Mode Control Byte	1-5
1.2.3	Floating-Point Status Register (FPSR)	1-5
1.2.3.1	Floating-Point Condition Code Byte	1-5
1.2.3.2	Quotient Byte	1-6
1.2.3.3	Exception Status Byte	1-6
1.2.3.4	Accrued Exception Byte	1-7
1.2.4	Floating-Point Instruction Address Register (FPIAR)	1-7
1.3	Supervisor Programming Model	1-8
1.3.1	Address Register 7 (A7)	1-10
1.3.2	Status Register	1-10
1.3.3	Vector Base Register (VBR)	1-11
1.3.4	Alternate Function Code Registers (SFC and DFC)	1-11
1.3.5	ACU Status Register (MC68EC030 only)	1-11
1.3.6	Transparent Translation/Access Control Registers	1-12
1.3.6.1	Transparent Translation/Access Control Register Fields for the M68030	1-12
1.3.6.2	Transparent Translation/Access Control Register Fields for the M68040	1-13
1.4	Integer Data Formats	1-14
1.5	Floating-Point Data Formats	1-15
1.5.1	Packed Decimal Real Format	1-15
1.5.2	Binary Floating-Point Formats	1-16
1.6	Floating-Point Data Types	1-17
1.6.1	Normalized Numbers	1-18

TABLE OF CONTENTS (Continued)

Paragraph Number	Title	Page Number
1.6.2	Denormalized Numbers	1-18
1.6.3	Zeros	1-19
1.6.4	Infinities	1-19
1.6.5	Not-A-Numbers	1-19
1.6.6	Data Format and Type Summary	1-20
1.7	Organization of Data in Registers	1-25
1.7.1	Organization of Integer Data Formats in Registers	1-25
1.7.2	Organization of Integer Data Formats in Memory	1-27
1.7.3	Organization of FPU Data Formats in Registers and Memory	1-30

Section 2
Addressing Capabilities

2.1	Instruction Format	2-1
2.2	Effective Addressing Modes	2-4
2.2.1	Data Register Direct Mode	2-5
2.2.2	Address Register Direct Mode	2-5
2.2.3	Address Register Indirect Mode	2-5
2.2.4	Address Register Indirect with Postincrement Mode	2-6
2.2.5	Address Register Indirect with Predecrement Mode	2-7
2.2.6	Address Register Indirect with Displacement Mode	2-8
2.2.7	Address Register Indirect with Index (8-Bit Displacement) Mode	2-9
2.2.8	Address Register Indirect with Index (Base Displacement) Mode	2-10
2.2.9	Memory Indirect Postindexed Mode	2-11
2.2.10	Memory Indirect Preindexed Mode	2-12
2.2.11	Program Counter with Displacement Mode	2-13
2.2.12	Program Counter Indirect with Index (8-Bit Displacement) Mode	2-14
2.2.13	Program Counter Indirect with Index (Base Displacement) Mode	2-15
2.2.14	Program Counter Memory Indirect Postindexed Mode	2-16
2.2.15	Program Counter Memory Indirect Preindexed Mode	2-17
2.2.16	Absolute Short Addressing Mode	2-18
2.2.17	Absolute Long Addressing Mode	2-18
2.2.18	Immediate Data	2-19
2.3	Effective Addresing Mode Summary	2-19
2.4	Brief Extension Word Format Compatibility	2-21
2.5	Full Extension Addressing Modes	2-22
2.5.1	No Memory Indirect Action Mode	2-24
2.5.2	Memory Indirect Modes	2-25
2.5.2.1	Memory Indirect with Preindex	2-25
2.5.2.2	Memory Indirect with Postindex	2-26
2.5.2.3	Memory Indirect with Index Suppressed	2-27

TABLE OF CONTENTS (Continued)

Paragraph Number	Title	Page Number
2.6	Other Data Structures	2-28
2.6.1	System Stack	2-28
2.6.2	Queues	2-29

Section 3
Instruction Set Summary

3.1	Instruction Summary	3-1
3.1.1	Data Movement Instructions	3-5
3.1.2	Integer Arithmetic Instructions	3-6
3.1.3	Logical Instructions	3-8
3.1.4	Shift and Rotate Instructions	3-8
3.1.5	Bit Manipulation Instructions	3-10
3.1.6	Bit Field Instructions	3-10
3.1.7	Binary-Coded Decimal Instructions	3-11
3.1.8	Program Control Instructions	3-11
3.1.9	System Control Instructions	3-12
3.1.10	Cache Control Instructions (MC68040)	3-14
3.1.11	Multiprocessor Instructions	3-14
3.1.12	Memory Management Unit (MMU) Instructions	3-15
3.1.13	Floating-Point Arithmetic Instructions	3-15
3.2	Integer Unit Condition Code Computation	3-17
3.3	Instruction Examples	3-20
3.3.1	Using the CAS and CAS2 Instructions	3-20
3.3.2	Using The MOVES Instruction	3-20
3.3.3	Nested Subroutine Calls	3-20
3.3.4	Bit Field Instructions	3-20
3.3.5	Pipeline Synchronization with the NOP Instruction	3-21
3.4	Floating-Point Instruction Details	3-21
3.5	Floating-Point Computational Accuracy	3-23
3.5.1	Intermediate Result	3-24
3.5.2	Rounding the Result	3-25
3.6	Floating-Point Postprocessing	3-27
3.6.1	Underflow, Round, Overflow	3-28
3.6.2	Conditional Testing	3-28
3.7	Instruction Descriptions	3-32

TABLE OF CONTENTS (Continued)

Paragraph Number	Title	Page Number
	Section 4 **Integer Instructions** (Listed Alphabetically)	
	Section 5 **Floating-Point Instructions** (Listed Alphabetically)	
	Section 6 **Supervisor (Privileged) Instructions** (Listed Alphabetically)	
	Section 7 **CPU32 Instructions** (Listed Alphabetically)	
	Section 8 **Instruction Format Summary**	
8.1	Instruction Format	8-1
8.1.1	Coprocessor ID Field	8-1
8.1.2	Effective Address Field	8-1
8.1.3	Register/Memory Field	8-1
8.1.4	Source Specifier Field	8-1
8.1.5	Destination Register Field	8-2
8.1.6	Conditional Predicate Field	8-2
8.1.7	Shift and Rotate Instructions	8-2
8.1.7.1	Count Register Field	8-2
8.1.7.2	Register Field	8-2
8.1.8	Size Field	8-4
8.1.9	Opmode Field	8-4
8.1.10	Address/Data Field	8-4
8.2	Operation Code Map	8-4

TABLE OF CONTENTS (Concluded)

Paragraph Number	Title	Page Number
	APPENDIX A **Processor Instruction Summary**	
A.1	MC68000, MC68008, MC68010 Processors	A-12
A.1.1	M68000, MC68008, and MC68010 Instruction Set	A-12
A.1.2	MC68000, MC68008, and MC68010 Addressing Modes	A-16
A.2	MC68020 Processors	A-17
A.2.1	MC68020 Instruction Set	A-17
A.2.2	MC68020 Addressing Modes	A-20
A.3	MC68030 Processors	A-21
A.3.1	MC68030 Instruction Set	A-21
A.3.2	MC68030 Addressing Modes	A-24
A.4	MC68040 Processors	A-25
A.4.1	MC68040 Instruction Set	A-25
A.4.2	MC68040 Addressing Modes	A-29
A.5	MC68881/MC68882 Coprocessors	A-30
A.5.1	MC68881/MC68882 Instruction Set	A-30
A.5.2	MC68881/MC68882 Addressing Modes	A-31
A.6	MC68851 Coprocessors	A-31
A.6.1	MC68851 Instruction Set	A-31
A.6.2	MC68851 Addressing Modes	A-31
	Appendix B **Exception Processing Reference**	
B.1	Exception Vector Assignments for the M68000 Family	B-1
B.2	Exception Stack Frames	B-3
B.3	Floating-Point Stack Frames	B-9
	Appendix C **S-Record Output Format**	
C.1	S-Record Content	C-1
C.2	S-Record Types	C-2
C.3	S-Record Creation	C-3